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The Effect of Exposure Time to Clean Room Air on Characteristic Parameters of Au/Epilayer $n-Si$ Schottky Diodes

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Abstract

A study has been made on determination and comparison of current-voltage (I-V) and capacitance-voltage (C-V) characteristics parameters of $Au/n-Si$ Schottky barrier diodes (SBDs) with and without thin native oxide layer fabricated on n-type Si grown by LPE (Liquid-phase Epitaxy) technique. The native oxide layer with different thicknesses on chemically cleaned on Si surface were obtained by exposing the surfaces to clean room air before evaporating metal. The native oxide thicknesses of samples D2, D3, D4 and D5 are in the form $D2 < D3 < D4 \leq D5$, depending on the exposing time. It has been seen that the values of barrier height Φ_b of samples D2(0.64 eV), D3(0.66 eV), D4(0.69 eV) and D5(0.69 eV) with the interfacial layer increased with increasing the exposure time and tended to that of the initial sample D1 (nonoxidezed sample, 0.74 eV), and thus also their I-V and C-V curves. The reverse current of sample D1 showed slight nonsaturating behavior. This "soft" behavior has been ascribed to the spatial inhomogeneity in the barrier heights at the MS interface. In particular, reverse bias curves of samples D2, D3, D4 and D5 have shown excellent saturation which may be attributed to the passivation of the semiconductor surface states by the native oxide layer which reduces the penetration of the wave functions of electron in the metal into the semiconductor. Especially, the I-V characteristics and experimental parameters of our devices are in agreement with recently reported results revealed by the pulsed surface photovoltage technique for the electronic properties of the HF-treated Si surface during initial oxidation in air.

1. Introduction

During recent years, application of surface and interface science techniques has shown clearly that interfaces formed between metals and semiconductors are complex regions whose physical properties depend on insensitivity of the preparation conditions of the surface because, in many cases, contact metals are deposited onto surfaces covered by unknown contaminants which may cause interface states and which can affect the mechanical and electrical properties of the contact, performance, reliability and stability of metal-semiconductor (MS) devices [1-19]. Therefore, the surface or interface states and interfacial oxide layer at the MS rectifying contact play an important role in the determination of the Schottky barrier height (SBH) and other characteristics parameters of the devices. The surface states can be viewed as electronic states generated by unsaturated dangling bonds of the surface atoms [1-16]. In the laboratory environment crystal surfaces are usually covered with layers of native oxides and organic contaminants, and surface states in the presence of these layers are modified and referred to as "interface states" [16]. In many cases, the barrier height obtained on cleaved and chemically prepared semiconductor surfaces indicate the presence of an interfacial layer. The effect of exposing cleaved and/or clean silicon surfaces to oxygen before forming the MS contacts has been investigated by many workers [9-16]. Archer and Atalla inspected the effect of exposing the surface to ambient oxygen for a few seconds before deposing the contact metal [9]. Turner and Rhoderick [10] estimated no difference in barrier heights on cleaved and etched surfaces for gold and nickel but a significant decrease on the etched surfaces for copper, silver and aluminium. In addition, the effect of the interfacial contamination on atomically clean Au and Ag and oxidized silicon contacts were investigated by Varma et al. [11]. In their paper, it was reported that the contamination reduced the mechanical strength of adhesion between the MS interface. Later on, Morita et al. [12] described the factors controlling the native oxide growth on Si surfaces (without any metal contact) in air and ultrapure water at room temperature. Recently, Dittrich et al. [13] and Angermann et al. [14] investigated the electronic properties (surface potential and surface state distribution) of the HF-treated Si surface by the pulsed surface photovoltage technique (SPV) during initial oxidation in air (the SPV measurement does not need any metal contact preparation). In spite of all these, and the nature of the M-S interfaces still remains controversial [1-5]. In addition, the characteristic parameters of the Schottky diodes formed exposing the epilayer-silicon surfaces to clean room air should also be investigated. Thereby, it is an important matter to consider together electrical characteristics of the SBDs with and without the interfacial oxide layer such that a comparison can be made. In this paper, we have investigated the effect of exposure time of the chemically cleaned (the RCA clean) n-type epilayer silicon surface to clean room air at room temperature before evaporating the metal on the I-V and C-V characteristics of the fabricated $Au/n-Si$ (epilayer) Schottky diodes. Thus, we have compared the parameters obtained from I-V and C-V characteristics of the $Au/n-Si$ (epilayer) fabricated on the epilayer Si without interfacial oxide layer with those of the $Au/n-Si$(epilayer) the with

the interfacial native oxide layer. In addition, for interpreting the experimental reverse bias $C^{-2}-V$ characteristics of the SBD with the interface states in equilibrium with the metal under the reverse bias condition, an expression for the capacitance C was obtained as a function of the applied voltage at sufficiently high frequency such that the interface states cannot follow the ac signal.

2. Theoretical Background

When the nonideal Schottky diode (MIS) is considered, it is assumed that the forward bias current the of device is due to thermionic emission current and be expressed as [5-8]

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right], \tag{1}$$

where

$$I_0 = AA^*\theta_n T^2 \exp\left(-\frac{q\Phi_b}{kT}\right), \tag{2}$$

is the saturation current density; Φ_b is the barrier height at zero bias; A^* is the effective Richardson constant and equals to $112A/cm^2K^2$ for n-type Si [20]; A the diode area; θ_n is the transmission coefficient the across the interfacial layer and is given by $\theta_n = \exp(-\chi_e^{1/2}\delta)$, where $\chi_e = 2/\hbar(2m_n\chi_c)^{1/2}$; m_n is the effective tunneling mass of electrons and χ_c is the effective barrier height presented by the thin interfacial layer. If the interfacial layer is extremely thin and is transparent to electrons, that is, $\chi_e^{1/2}\delta << 1$, then $\theta_n \approx 1$ [6]. n is an ideality factor and is a measure of conformity of the diode to pure thermionic emission and is contained in the slope of the straight line region of the forward bias I-V characteristics through the relation

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)}. \tag{3}$$

If n is equal to one, pure thermionic emission occurs. However, n usually has a value greater than unity.

When the interface states is entirely governed with the semiconductor Fermi level in the reverse bias and the frequencies are sufficiently high that the interface states cannot follow an ac signal, the slope of the $C^{-2}-V$ plot for an MIS (metal-interfacial layer-semiconductor) diode is expressed as obtained by Fonash [17]:

$$\frac{dC^{-2}}{dV} = -\frac{2}{e\epsilon_s A^2 N_d}\left[\frac{C_{sc}+C_I}{(1+\alpha)C_I + C_{sc}}\right], \tag{4}$$

where

$$\alpha = \frac{q^2 N_{sb}\delta}{\epsilon_i}, \tag{5}$$

$C_I = \epsilon_i/\delta$ is the capacitance of the interfacial oxide layer; N_{sb} is the density of the interface states in equilibrium with the semiconductor and is assumed to be constant through the band gap; q is the electronic charge; N_d is the doping concentration of the n-type semiconductor; ϵ_s and ϵ_i are the permittivities of the semiconductor and the interfacial layer; and δ is the thickness of the interfacial layer. Equation (4) has the physically acceptable interpretation that the equivalent circuit of device will be just the oxide layer and the depletion capacitance in series. If $C_I >> C_{sc}$, Eqn. (4) reduces to

$$\frac{dC^{-2}}{dV} = -\frac{2}{e\epsilon_s A^2 N_d}\frac{1}{(1+\alpha)}. \tag{6}$$

Under these assumptions, the slope of high frequency $C^{-2} - V$ curve of an MIS diode is still constant and differs from that of an corresponding ideal MS diode by a factor of $1/(1+\alpha)$. When N_{sb} varies appreciably over the band gap, Eqn. (5) is still valid; however, the C^{-2} vs V curve will no longer be linear [17]. Furthermore, Fonash [17] shows that the intercept V_0 of the high frequency $C^{-2} - V$ curve is given by

$$V_0 = (1+\alpha)V_{bo}, \tag{7}$$

when δ and N_d are sufficiently small.

3. Experimental Procedure

The n-type Si wafer used for the $Au/n-Si$ Schottky diodes was about $18\mu m$ thickness having a phosphorus-doped layer with 2 Ω-cm resistivity grown by LPE (Liquid-phase Epitaxy) technique on 0.01 Ω-cm (antimony-doped) n^+ substrate (100). The wafer was chemically cleaned using the RCA cleaning procedure [i.e., a 10 min boil in $NH_4 + H_2O_2 + 6H_2O$ followed by a 10 min boil in $HCl + H_2O_2 + 6H_2O$] with the final cleaning rinse in diluted HF for 30s, and then rinsed by ultrasonic vibration in DI water and dried by high-purity nitrogen. After the ohmic contact to back surface of the wafer was made by evaporating $Au - Sb$, the wafer was cut into pieces of $5 \times 5mm^2$. One of them was immediately inserted into the evaporation chamber to form intimate Schottky contacts without the native oxide layer. This sample will be called D1. However, it has been reported that even diodes made by cleaving in a stream of metal in high vacuum have a very thin effective native oxide layer [1-15, 19-21]; but for convenience, we refer this sample as a nonoxidized sample in this paper [1-15, 19-21]. Before the remaining pieces with ohmic contact were made into Schottky contacts, one of them was exposed to clean room air at room temperature for one day (sample D2) to obtain a native oxide layer on the clean Si surface (so as to observe nonideality due to the native interfacial layer); the third piece for three days (sample D3); the forth piece for a week (sample D4); and the fifth piece for two weeks (sample D5). The clean room air is characterized by an average temperature of $25°C$ and an average humidity of 40 %. It is well known that the interfacial layer thickness between metal and semiconductor is dependent on

exposure time of the semiconductor surface to residual gases in the case of chemically cleaned substrates [4, 5, 12-16]. The layer-by-layer growth of the native oxide layer which is inevitably present on chemically prepared semiconductor surfaces thus occurs even when it is exposed to clean room air [4, 5, 12-16]. The Schottky contacts were formed by evaporating Au as dots with diameter of about 1 mm onto all the sample surfaces. Thus, the $Au/n-Si$ samples with and without the interfacial layer were obtained. All evaporation processes were carried out in a turbo molecular fitted vacuum coating unit at about 10^{-6} mbar. The dark current-voltage characteristics were measured using a HP 4140B picoampermeter/ I-V plotter. The dark small signal AC capacitance measurements as a function of the applied voltage were made using a HP 4280A capacitance meter/C-V plotter. The measurements were made at the room temperature.

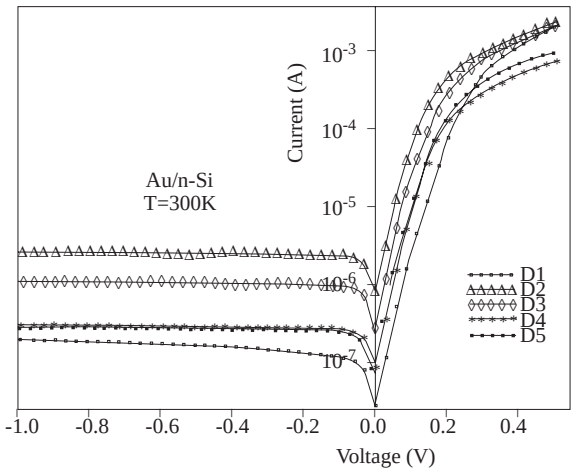

Figure 1. The forward and reverse bias current vs voltage characteristics of the $Au/n-Si$ Schottky barrier diodes at the room temperature, curve D1 corresponds to nonoxidized sample D1, and curves D2, D3, D4 and D5 to samples D2, D3, D4 and D5 with the interfacial native oxide layer.

4. Results and Discussion

In order to compare theoretical predictions with experimentally measured Schottky barrier diodes (SBDs) it is desirable to consider only those measurements made on unreactive metal-semiconductor (MS) interfaces where interdiffusion across the interface is minimal. As such, we used gold metal as the rectifying contact, as it is far less reactive [1, 5]. Curves D2, D3, D4 and D5 in Figure 1 show the experimental semilog forward and reverse bias characteristics of the $Au/n-Si$ SBHs (D2, D3, D4 and D5) with

the interfacial native oxide layer with the forward saturation currents $I_{f,o}$ of $1.51 \times 10^{-6}, 6.00 \times 10^{-7}, 1.71 \times 10^{-7}$ and $1.92 \times 10^{-7} A$, respectively. Curve D1 in Figure 1 shows the I-V characteristics of sample D1 with $I_{f,o} = 3.47 \times 10^{-8} A$. The values of the SBHs Φ_b of the samples were calculated from the y-axis intercepts of the semilog forward and reverse bias I-V plots according to Eqn. (2). The value of 0.74 eV for Φ_b for sample D1 is almost the same as value of 0.74 eV obtained for $Au/n-Si$ made by evaporation on etched silicon in CP4-A from the I-V characteristics by Varma et al. [11]. Turner and Rhoderick [10] found no difference in barrier heights on cleaved and etched surfaces for gold and nickel but a significant decrease on etched surfaces for copper, silver and aluminum. The linear regions interval of the forward bias curves and the values of $I_{f,o}$ and Φ_b of samples D2, D3 and D4 were found to increase with increasing exposure time to the room air and tended to those of sample D1. The ideality factor values of samples were obtained from the slopes of the linear regions of the forward plots with the help of Eqn. (3). The obtained experimental values of the parameters are given in Table 1. As can be seen in Table 1, the ideality factor values of 1.06, 1.10, 1.10 and 1.10 for samples D2, D3, D4 and D5, respectively, show that the devices obey not an ideal Schottky diode but a MIS configuration and that the interface states are in equilibrium with the semiconductor over the applied voltage range [5, 8, 21, 24, 25]. Thus, the departures from ideal behavior due to the interfacial layer thickness may be described by an n-value which increases with increasing oxide thickness. The fact that n values for samples D2, D3, D4 and D5 and the concavity of the non-linear regions in their forward logarithmic I-V curves increase with increasing exposure time to the room air with respect to those of initial sample D1, indicates that the interfacial layer thicknesses δ of samples increases with increasing exposure time. However, it is clearly visible from n values and the I-V curves of the samples with oxide layer that tunneling takes place readily through the very thin native oxide layer. We can confidently assume the sample D1 to have an almost ideal I-V characteristic with ideality factor value of 1.01, which can be explained solely in terms of image-force lowering [21-23]. Near ideal rectification properties are possible ($n \approx 1$) provided that the interface states (HF-induced extrinsic states [12-14]) are in equilibrium with those in the metal for small voltages. In the calculation the voltage drop in the oxide layer is negligibly small, but at large forward voltages the interface states are in equilibrium with the semiconductor [5, 8, 21]. For smaller values of Φ_b, the interface states (another group of the interface states always observed during oxidation of HF-treated Si surfaces in air [12-14]) will be in equilibrium with the semiconductor even at low voltages [5, 8, 21].

The barrier height Φ_b value of 0.74 eV for sample D1, which is the nonoxidized sample immediately inserted into the evaporation chamber without exposing to clean room air, is larger than those for the samples with the native oxide layer. This case is attributed to the passivation of the cleaned Si surface after HF treatment, as pointed out in experimental section. Hydrogen plays an important role for the electrical passivation of the HF-treated Si surface, similar to the trap passivation at the Si/SiO_2 interface [1-3, 12-15]. That is, Si atoms at the cleaned Si wafer surface are terminated by hydrogen.

The H termination results in well ordered, atomically flat surfaces exhibiting terraces of thousands of angstrom wide [12-14]. As can be seen in Table 1, Φ_b value of 0.64 eV for sample D2 (exposed to air for one day) is lower than those for samples D3 (for three days, 0.66 eV), samples D4 (for 1 week, 0.69 eV) and samples D3 (for two weeks, 0.69 eV). This case may also be ascribed to characteristics that oxygen species break Si-Si bonds to produce Si-O bonds, with the remaining Si-H bonds to cause hidrophobic behavior [12-14]. That is, HF induced extrinsic states decrease after an initial phase of 24h, while in other groups the extrinsic states additionally appear such as Si-O bonds; and their maximum concentration, reached after 7 days, is followed by a slow decrease during further exposure to air [12-14]. Likewise, as can be seen from the above values and Table 1, the pattern that the values of Φ_b for the samples with native oxide layer increase with increasing deposition time in air, and tend to 0.74 eV in the case of the initial sample D1, may be explained as follows: During further storage in air, the oxygen species are produced at native oxide surfaces by the coexistence of O_2 and H_2O, or Si-O bonds are produced by the coexistence $O_2(O)$ and $H_2O(OH)$ near Si-Si bonds. The $Si-Si$ bonds of the underlayer Si are broken to produce Si-O bonds after all of the Si atoms in the overlayer are oxidized; i.e., the overlayer structure converts to the amorphous phase, resulting in layer-by-layer oxide growth as seen in Figure 16 of Ref. [12], which is related to a model of native oxide growth in air. Thus the surface state distribution becomes more and more like a Si/SiO_2 interface after long exposure to air. Stabilization of the Si/SiO_2 interface is confirmed with the ideality factor values of 1.10, 1.10 and 1.10 for samples D3, D4 and D5, respectively. This case is clearly seen also from the I-V curves of samples D4 and D5. Especially, the I-V characteristics and experimental parameters of our Au/nSi SBDs are in agreement with recently reported experimental results [12-14] revealed by the pulsed surface photovoltage (SPV) technique [13, 14] used to examine the electronic properties of the HF-treated Si surface during initial oxidation in air. The SPV measurements do not need any metal contact to the semiconductor under consideration.

Figure 2 shows the Fermi level position as a function of exposure time of the wafers to air at room temperature. This figure was drawn with the help of the barrier height values obtained from the forward I-V characteristics of the samples. The exposure time ranges from 24h (1440 min) to 336h (20160 min). Two regions can be seen which are characterized by a rapidly decreasing (A) and constant Fermi level (B). We connect the regions A and B to the formation of a Si/SiO_2 interface (region A, where the electronic properties of the surface change drastically) and to the stabilization of the Si/SiO_2 interface (region B, where the electronic properties are similar to the Si/SiO_2 interface), respectively, depending on the above explained dynamics.

The change of the Fermi level in the exposure time range 24-336h is in agreement with results determined by pulsed surface photovoltage technique in Figure 4 of Ref. [13]. The obtained characteristics parameters of our Schottky diodes fabricated using the same metal (Au) and semiconductor (n-Si), depending on the electronic properties of the surface change, confirm Barden's model as well [18].

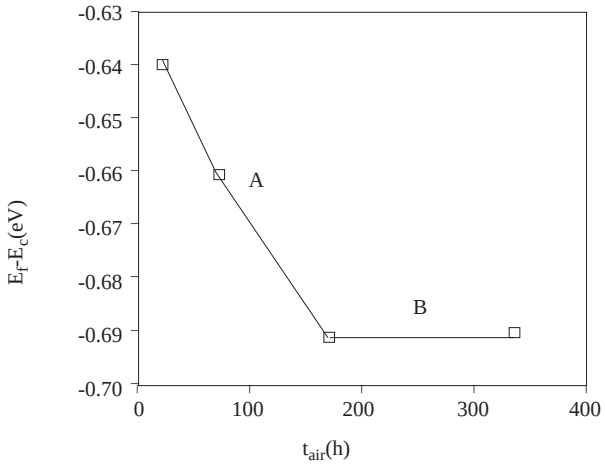

Figure 2. The Fermi level position as a function of exposure time to air for the wafers at room temperature.

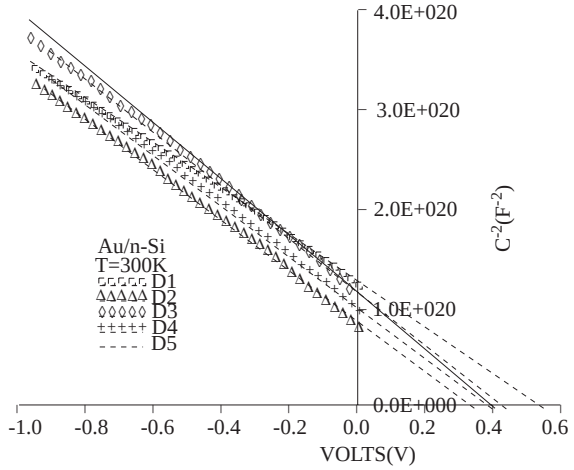

Figure 3. The reverse bias C^{-2} vs V curves at 1 MHz of $Au/n-Si$ Schottky diodes at the room temperature, curve D1 corresponds to nonoxidized sample D1, and curves D2, D3, D4 and D5 to samples D2, D3, D4 and D5 with the interfacial native oxide layer.

According to this model, if the density of localized surface states having energies distributed in the semiconductor energy gap is sufficiently high, a double layer at the

surface of the semiconductor is formed from the net charge of electrons in surface states and space charge of opposite sing. This double layer will tend to make the work function independent of the height of the Fermi level in the interior of the semiconductor, and the rectification characteristics of a metal-semiconductor (MS) contact are then practically independent of the work function.

Moreover, we observe the "soft" or slight nonsaturating behavior in reverse bias (curve D1 in Figure 1) of the initial sample D1 (nonoxidized). This "soft" behavior may be due to an additional bias-dependent barrier lowering mechanism of the SBHs as compared to those of samples D2, D3, D4 and D5 with the interfacial layer, the curves of which showed the exact saturation. Consequently, the fact that the Φ_b values of samples D2, D3, D4 and D5 with the interfacial layer increase with increasing the exposure time to the room air and tended to that of the initial sample D1. Especially, their reverse bias curves with exact saturation can be attributed to the passivation of the semiconductor surface states by the insulating native oxide layer, which reduces the penetration of the wavefunctions of electron in the metal into the semiconductor.

The $C^{-2}-V$ characteristics presented in the Figure 3 were measured at frequency of 1 MHz, at room temperature without illumination so that the interface states are unable to respond to the 1 MHz signal. The linearity of the $C^{-2}-V$ plot excludes the possibility of the interface state participation. This will occur when the time constants for the most of the interface states are too long to response to the applied *ac* signal. The intercept voltage; V_0, values of samples D2, D3, D4 and D5 are deduced as 0.58, 0.36, 0.45, 0.41 and 0.42 Volts, respectively, from $C^{-2}-V$ curves (Figure 3), and thus also the SBH values of 0.83, 0.61, 0.70, 0.66 and 0.67 eV, respectively, when the above values of V_0 are added to Fermi energy V_n for 0.25 eV for our sample Si. The value of 0.83 eV for sample D1 is almost the same as the value of 0.82 eV obtained for $Au/n-Si$ from the C-V characteristics by Turner et al. [10] and Varma et al. [11]. These values are given in Table 1. As have been seen in Table 1 for the nonoxidized sample D1, owing to the different nature of the C-V and I-V measurement techniques [3, 5, 23, 26], the SBH value measured by the $C^{-2}-V$ technique (0.83 eV) exceeds that derived from I-V technique (0.74 eV). This discrepancy can be attributed to the presence of the interface states [26]. The C-V method gives average SBH for the entire SB diode [3, 26]. The dc current across the interface depends exponentially on Φ_b and the current flows preferentially through the barrier minima [3, 26]. The reason for relatively high difference between the SBH values measured by the $C^{-2}-V$ technique for the nonoxidized sample D1 and those measured by the same technique for D2, D3 and D4 with the native oxide layer originates from the presence of the interfacial layer as well as the interface states [5, 17, 24]. The presence of the interfacial parameters will alter the $C^{-2}-V$ plot intercept voltage even if the measurements are made at a high frequency [5, 17, 24]. At a given bias, if the Fermi level does not coincide with the neutral level, there will be a net interface state charge at the surface due to the interface states, and these charges will give rise to an additional field in the oxide layer. This will result in a larger voltage drop across the oxide layer than would be experienced if no interface states were present, and the values of the intercept voltage,

and thus the SBHs, differ from expected values [2, 5]. The differences between the values of the SBHs obtained from the I-V and C-V methods for samples D2, D3, D4 and D5 may be ascribed to interface contamination which leads to a reduction of the mechanical strength of the adhesion between the metal and semiconductor [5, 11]. As can be seen from Figure 3, the slope values of $C^{-2}-V$ plots of $2.44\times10^{20}, 2.60\times10^{20}, 2.46\times10^{20}$ and $2.75\times10^{20}F^{-2}/V$ for the MIS diodes D2, D3, D4 and D5 depending on its ideality factor are respectively different from the slope value of $2.20\times10^{20}F^{-2}/V$ for MS diode (the nonoxidized sample D1) confirming the especially Eqns. (5) and (7) which represents the case where the population of the interface states entirely governs by the metal Fermi level and the frequency is sufficiently high that these states cannot follow the ac signal.

Table 1. Experimental values of parameters obtained from I-V and $C^{-2}-V$ characteristics of the $Au/n-Si$ SBDs fabricated on epilayer $n-Si$ with and without the native oxide layer, Φ_{bf}: the forward bias barrier height, Φ_{br}: the reverse bias barrier height, $\Phi_{b,cv}$: the barrier height from C-V characteristics

Diodes	$n=1/c_2$	Φ_{bf} (eV)	Φ_{br} (eV)	$\Phi_{b,cv}$ (eV)	$V_{0,cv}$ (V)
D1	1.01	0.73	0.71	0.83	0.58
D2	1.02	0.64	0.63	0.61	0.36
D3	1.10	0.66	0.65	0.70	0.45
D4	1.10	0.69	0.69	0.66	0.41
D5	1.10	0.69	0.69	0.67	0.42

In conclusion, the I-V characteristics and experimental parameters of the Au/nSi SBDs are in agreement with recently reported experimental results revealed by the pulsed surface photovoltage technique (SPV). It has been seen that the characteristics parameters of samples D2, D3, D4 and D5 have increased with increasing exposure time to room air and that the I-V and C-V characteristics and Φ_b values tended to those of sample D1.

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